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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/505,382	02/16/2000	Roy R. Faget	10001840-1	6474

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	16

DATE MAILED: 10/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PRE

Office Action Summary	Application No.	Applicant(s)	
	09/505,382	FAGET, ROY R.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This communication is responsive to Request for Reconsideration, filed 9/16/2003.

2. Claims 1-20 are pending in this application. Claims 1 and 11 are independent claims. This action is made final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-6, 8, 10-16, 18, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Vatinel (U.S. 6,317,763).

Re claim 1, Vatinel discloses a logic circuit in Figure 1 for use in a multiplexer to shift the input data (col.. 1 lines 19-22) comprising: a plurality of logic gates (nine rows wherein each row comprising transistors) for receiving data input (upper portion of 6 and col. 1 lines 29-31) and control signals (lower portion of 6 and col. 1 lines 37-39) wherein each data input line has a one to one correlation to a single data transistor (each input data is connecting to a buffer as seen in part 6 of Figure 1 wherein the buffer is inherently comprised transistors but has only one transistor interfaces with the input data line); and a plurality of shared data lines (the data bus from outputs of the buffers to all plurality of

logic gates) connecting logic gates the shared data lines providing a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates (e.g the second input data is connected to an buffer and the output of buffer is connected to all other logic gates across the array), wherein the logic gates shift data received at the data inputs based upon the control signals (col. 1 lines 42-44) and the connections of the shared data lines to produce a shifted data output (output data 5), and wherein all of the plurality of logic gates share a single data transistor for each data input (all the parts of row logic gates is are connected to the output of input data buffer).

Re claim 2, Vatinel further discloses the above logic circuit in Figure 1 wherein each of the logic gates includes first (shift) and second (un-shift) stages shift operation.

Re claim 3, Vatinel further discloses the above logic circuit in Figure 1 wherein each of the logic gates includes control inputs for receiving two set of shift control signals (the control signal 7 is inputted into the logic gates by 4) for the first and second stages of shifting.

Re claim 4, Vatinel further discloses the above logic circuit comprising another plurality of shared data lines (data bus from output of buffers 6 to rows of logic gates 8) for providing data inputs to the second stage of shifting for the second shifting operation.

Re claim 5, Vatinel further discloses the above logic circuit in Figure 1 wherein the plurality of shared data lines connect adjacent logic gates (the shared data bus connect all the parts of row of logic gates as a step) among the plurality of logic gates.

Re claim 6, Vatinel further discloses the above logic circuit in Figure 1 wherein each of the logic gates receives as one of the data inputs (input data 6) as a primary data line.

Re claim 8, Vatinel further disclose the above logic circuit in Figure 1 wherein each of the logic gates control by the control signals (4) and the logic gates including a plurality of transistors (8).

Re claim 10, Vatinel further discloses the above logic circuit in Figure 1 wherein each of the shared data lines connect one of the logic gates with a plurality of the logic gates (in Figure 1, the share data bus from input data buffer connects all the plurality of the logic gates together at different parts).

Re claim 11, it is a method claim of claim 1. Thus, claim 11 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 12, it is a method claim of claim 2. Thus, claim 12 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 13, it is a method claim of claim 3. Thus, claim 13 is also rejected under the same rationale in the rejection of rejected claim 3.

Re claim 14, it is a method claim of claim 4. Thus, claim 14 is also rejected under the same rationale in the rejection of rejected claim 4.

Re claim 15, it is a method claim of claim 5. Thus, claim 15 is also rejected under the same rationale in the rejection of rejected claim 5.

Re claim 16, it is a method claim of claim 6. Thus, claim 16 is also rejected under the same rationale in the rejection of rejected claim 6.

Re claim 18, it is a method claim of claim 8. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 8.

Re claim 20, it is a method claim of claim 10. Thus, claim 20 is also rejected under the same rationale in the rejection of rejected claim 10.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7 and 17 are rejected under 35 U.S.C. 103(a) as being obvious over Vatinel (U.S. 6,317,763) in view of Hervin et al. (U.S. 5,961,575).

Re claim 7, Vatinel does not disclose each of the logic gates receives a clocking signal for enabling the logic gates to feed data. However, Hervin et al. disclose in Figure 3 a system clock is used to trigger the data for inputting and shifting. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a clock signal as seen in Hervin et al.'s invention into Vatinel's Figure 1 because it would enable all the data synchronize properly for shifting (Figure 3).

Re claim 17, it is a method claim of claim 7. Thus, claim 17 is also rejected under the same rationale in the rejection of rejected claim 7.

7. Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being obvious over Vatinel (U.S. 6,317,763).

Re claim 9, Vatinel does not disclose each of the logic gates provides complementary outputs as the shifted data output. However, the examiner takes an office notice that it is well known the logic gates would provides a complementary outputs. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to provide a complementary outputs (x and bar(x)) in Vatinel's Figure 1 because it would allow the system to easily manipulate the output signals.

Re claim 19, it is a method claim of claim 9. Thus, claim 19 is also rejected under the same rationale in the rejection of rejected claim 9.

Response to Arguments

8. Applicant's arguments filed 9/16/2003 have been fully considered but they are not persuasive.

a. The applicant argues in pages 4-5 for claim 1 that the cited reference by Vatinel does not disclose or suggest the limitations cited in claim 1. In particular, Vatinel does not provide for one to one correlation between a data input line and single data transistor because each data input is inputted into nine p-feds in parallel. Second, the circuit shown in Figure 1 does not share data transistors for each data input.

The examiner respectfully submits that the Office rejection for claim 1 by Vatinel is clearly recited above. The applicant may mis-interpret the cited prior art

because Figure 1 clearly discloses the input data (upper portion of part 6) connect to nine input buffers (little triangles) instead of connecting directly into the nine p-feds (first row of transistors in Figure 1) in parallel. Buffers are well-known in the art that comprises transistors to drive the input signal. Therefore, Vatinel does provide in Figure 1 a circuit with one to one correlation between a data input line (upper portion of part 6) and a single data transistor (an interfaced transistor within the buffers). This might correspond to part 40 in Figure 2A in the present application. The data bus connects the output of buffers to each individual row of transistors (row of logics) is the share data line. As clearly shown in Figure 1, there are only nine share interfaced transistors receiving input data from part 6 (transistors within buffers that receiving input data) and distributed to all logics using the share data lines (share data bus that connects the output of buffers to all the logics).

9. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., cited limitations "The other data inputs are received from adjacent or other logic gates using shared data lines" in argument page 4 lines 29-31) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Chat C. Do
Examiner
Art Unit 2124

October 1, 2003

CHUONG DINH NGO
PRIMARY EXAMINER